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10/534,343	07/18/2005	Anthony Spencer	0120-032	4839

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POTOMAC PATENT GROUP PLLC
P. O. BOX 270
FREDERICKSBURG, VA 22404

EXAMINER	
CLARK, MAXWELL A	
ART UNIT	PAPER NUMBER
2616	

NOTIFICATION DATE	DELIVERY MODE
07/10/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

tammy@ppglaw.com

Office Action Summary	Application No.	Applicant(s)	
	10/534,343	SPENCER, ANTHONY	
	Examiner	Art Unit	
	MAXWELL A. CLARK	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *05/09/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

A patent abstract should be such as to enable the reader thereof, regardless of his or her degree of familiarity with patent documents, to determine quickly from a cursory inspection of the nature and gist of the technical disclosure and should include that which is new in the art to which the invention pertains, see MPEP § 608.01(b).

The abstract is merely a recitation of the claims. Appropriate correction is required.

2. Claims 1 and 9 are objected to because of the following informalities: "Generating from a said data packet a record portion of predetermined fixed size and containing information about the packet" should be changed to "Generating from said data packet a record portion of predetermined fixed size and containing information about the packet". Appropriate correction is required.

3. Claim 9 is objected to because of the following informalities: "queueing" should be changed to "queuing".

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

6. Regarding claims 1 and 9,

a. "with each data portion having no connection with any other" is indefinite because it is unclear what is meant by the limitation "any other", it is not apparent in what respect "each data portion has no connection with any other".

b. It is unclear what is meant by the phrase "the data in the packet being in a data portion" and what limits are being sought for protection.

c. "Generating from a said data packet a record portion of predetermined fixed size and containing information about the packet" is indefinite because the specification does not explicitly define the record portion but merely states that a

record packet contains information about its respective data packet and is of a smaller fixed size.

d. The phrase "lower address bandwidth" is indefinite. It is unclear what applicant considers the limitation.

7. The term "relatively large" and "relatively small" in claims 2 and 9 are relative terms which renders the claims indefinite. The terms "relatively large" and "relatively small" is not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Asten et al. (US 2003/0174699 A1) in view of Rege et al. (USPN 5,390,299).

Regarding claim 1, Van Asten discloses queuing variable size data packets in a communication system (abstract, wherein storing and retrieving variable size packets in a high-speed packet memory corresponds to queuing variable size data packets in a communication system), generating from a said data packet a record portion of predetermined fixed size and containing information about the packet (¶0026, wherein the MCP for each group of cells (the associated MCP), each MCP having N memory module identifiers to record the order in which said cells of said each group are stored in each of the selected different one of the N memory modules; ¶0024, wherein the N memory modules are for storing fixed size cells each correspond to the record portion of predetermined fixed size and containing information about the packet), the data in the packet being in a data portion (examiner takes official notice that data in a packet is in a data portion); storing data portions in independent memory locations in a first memory with each data portion having no connection with any other (¶0061, wherein storing each cell, which belongs to the same group of cells, in a selected different one of the N memory modules, i.e. different memory location in a first memory, at the same memory address corresponds to storing data portions in independent memory locations in a first memory with each data portion having no connection with any other), storing record portions in one or more managed queues in a second memory (¶0063, wherein storing the MCP in an MCP storage at an MCP address corresponds to storing record portions in one or more managed queues in a second memory), the memory locations in the first memory are arranged in blocks having a plurality of different sizes and the memory locations are allocated to the data portions according to the size of the data portions

(¶0154 wherein the same segmented packet containing more than N switch cells, then additional MCPs and DRAM storage locations are assigned. The number of addresses required to store an entire segmented packet is equal to the number of switch cells divided by M and rounded up. For example a 1500 byte IP data packet may be segmented into a segmented packet of 26 switch cells. If N=5, a total of 6 MCPs would required, and 6 addresses assigned, to store the switch cells deriving from such an IP packet which corresponds to the memory locations in the first memory are arranged in blocks having a plurality of different sizes and the memory locations are allocated to the data portions according to the size of the data portions). Van Asten does not expressly disclose a second memory having a fixed size memory. However, Van Asten does disclose the size of the record portions are fixed in size (¶0024, wherein the plurality of N memory modules for storing fixed size cells which are segments of a variable size packet divided into X cells corresponds to disclose the size of the record portions are fixed in size). It would have been obvious to one of ordinary skill in the art at the time of the application to disclose the memory having fixed size memory in order to accommodate for the fixed sized cells. Also, Van Asten does not expressly disclose the first memory larger that the second. However, Van Asten does disclose the use of different memories for the multi-cell pointers and data cells. It would have been obvious to one of ordinary skill in the art at the time of the application to disclose multi-cell pointer memory smaller than data memory because it is well known that the data portion requires more memory that the multi-cell pointer data.

Regarding claim 2, Van Asten discloses two sizes of memory location in the first memory arranged in two said blocks, one of a size to receive relatively small data portions and the other of a size to receive relatively large data portions, and wherein data portions that are too large to be stored in a single memory block are stored as linked lists in a plurality of blocks (¶0007- ¶0008, wherein a large packet switch comprises several port cards and a switch fabric. The port cards in the large packet switch differ in a number of details from the port cards of the small packet switch. In the large packet switch, there is no single shared packet memory (as in the small packet switch); rather, each port card contains a separate packet memory which corresponds to two sizes of memory location in the first memory arranged in two said blocks, one of a size to receive relatively small data portions and the other of a size to receive relatively large data portions, and wherein data portions that are too large to be stored in a single memory block are stored as linked lists in a plurality of blocks). with pointers pointing to the next block but without any pointers pointing from one data portion to the next data portion of the packet (¶0071 wherein recognizing the segmentation of packets provides switching behavior (selective read) rather than FIFO behavior to keep track of cell storage locations; ¶0078, fig7, wherein multi-cell pointer management structure each corresponding to pointers pointing to the next block but without any pointers pointing from one data portion to the next data portion of the packet).

Regarding claim 3, Van Asten discloses the sizes of the memory locations in the blocks are matched to the most commonly occurring sizes of data packets in the communication system (¶0013, wherein the fixed size packets (cells) correspond to the

most commonly occurring sizes of data packet, since they are commonly set to the fixed size, and wherein the packet memories based on the cell size corresponds to the memory location in the blocks matching the commonly occurring sizes of the data packets).

Regarding claim 4, Van Asten discloses allocating the memory locations in said first memory from a pool of available addresses provided to it in batches from a central pool of available addresses (¶025, wherein the memory address being selected from a sub-set, i.e. pool, of N memory addresses corresponds to allocating the memory locations in said first memory from a pool of available addresses provided to it in batches from a central pool of available addresses).

Regarding claim 5, Van Asten discloses memory blocks segregated into a plurality of memory channels, the method further comprising allocating addresses to data portions sequentially across channels whereby to spread the storage of data portions across the channels (¶0030, wherein the number of memory modules in the plurality of N memory modules may vary depending on the application and is equal to N=5 in the embodiment of the invention wherein the variable size packet may be divided into different number X of cells depending on the cell size, conveniently X ranging from X=1 to about 200 corresponds to memory blocks segregated into a plurality of memory channels, the method further comprising allocating addresses to data portions sequentially across channels whereby to spread the storage of data portions across the channels).

Regarding claim 6, Van Asten discloses reading the data portions from the first memory in pipelined manner by a data retrieval unit adapted to instruct a memory block to read out a data portion without having to wait for the previous read to be completed, and releasing the address location from the first memory (¶0170, fig.8, wherein providing a pipelined system comprised of the read queues 608, read command queues 610, and the associated control logic in the read-write control 300 permits many switch cells to be requested and retrieved from the DRAM storage in parallel and re-ordered in separate queues, without stalling the flow of cells so that the read operation is not a single pipeline of requests and switch cell deliveries, but multiple pipelines are running in parallel corresponds to reading the data portions from the first memory in pipelined manner by a data retrieval unit adapted to instruct a memory block to read out a data portion without having to wait for the previous read to be completed, and releasing the address location from the first memory).

Regarding claim 7, Van Asten discloses a large packet switch, the bandwidth available through the switch fabric usually greater than the bandwidth of the line interface in the port card, in order to accommodate the fluctuating packet traffic without the loss of packets. Van Asten does not expressly disclose an overflow situation when there is insufficient memory for a received packet wherein the data portion is discarded. However, Rege claims discarding one of said data packets when said one of said data packets is received and said packet buffer memory has insufficient free space to store said one of said data packets and a discard counter, i.e. record portion, to store a

discard count of the number of said data packets that are discarded, see claim 9, for the purpose handling an inevitable situation of overflow.

Regarding claim 8, Van Asten discloses reading the address locations from a bitmap of addresses (fig. 10-806, wherein get next read command address A, count K corresponds to reading the address locations from a bitmap of addresses) when a memory location is released after the data stored therein has been read out (fig. 10-818, wherein release MCP corresponds to memory location is released after the data stored therein has been read out, i.e. cell put on read queue, fig. 10-812), the address of the released memory location is sent directly to the pool (fig. 10-818, wherein address is placed on a free list corresponds to the address of the released memory location is sent directly to the pool).

Regarding claim 9, Van Asten discloses a memory hub for queuing received data packets (abstract, wherein storing and retrieving variable size packets in a high-speed packet memory corresponds to queuing variable size data packets in a communication system), arrivals block, adapted to generate from a said data packet a record portion of predetermined fixed size and containing information about the packet(¶0026, wherein the MCP for each group of cells (the associated MCP), each MCP having N memory module identifiers to record the order in which said cells of said each group are stored in each of the selected different one of the N memory modules; ¶0024, wherein the N memory modules are for storing fixed size cells each correspond to the record portion of predetermined fixed size and containing information about the packet), the data in the packet being in a data portion (examiner takes official notice that data in a packet is in a

data portion); a first memory for storing data portions in independent memory locations, with each data portion having no connection with any other (¶0061, wherein storing each cell, which belongs to the same group of cells, in a selected different one of the N memory modules, i.e. different memory location in a first memory, at the same memory address corresponds to storing data portions in independent memory locations in a first memory with each data portion having no connection with any other); storing record portions in one or more managed queues in a second memory (¶0063, wherein storing the MCP in an MCP storage at an MCP address corresponds to storing record portions in one or more managed queues in a second memory); the memory locations in the first memory are arranged in blocks having a plurality of different sizes and the memory locations are allocated to the data portions according to the size of the data portions (¶0154 wherein the same segmented packet containing more than N switch cells, then additional MCPs and DRAM storage locations are assigned. The number of addresses required to store an entire segmented packet is equal to the number of switch cells divided by M and rounded up. For example a 1500 byte IP data packet may be segmented into a segmented packet of 26 switch cells. If N=5, a total of 6 MCPs would required, and 6 addresses assigned, to store the switch cells deriving from such an IP packet which corresponds to the memory locations in the first memory are arranged in blocks having a plurality of different sizes and the memory locations are allocated to the data portions according to the size of the data portions). Van Asten does not expressly disclose a second memory having a fixed size memory. However, Van Asten does disclose the size of the record portions are fixed in size (¶0024, wherein the plurality of

N memory modules for storing fixed size cells which are segments of a variable size packet divided into X cells corresponds to disclose the size of the record portions are fixed in size). It would have been obvious to one of ordinary skill in the art at the time of the application to disclose the memory having fixed size memory in order to accommodate for the fixed sized cells. Also, Van Asten does not expressly disclose the first memory larger that the second. However, Van Asten does disclose the use of different memories for the multi-cell pointers and data cells. It would have been obvious to one of ordinary skill in the art at the time of the application to disclose multi-cell pointer memory smaller than data memory because it is well known that the data portion requires more memory that the multi-cell pointer data.

Regarding claim 10, Van Asten discloses a memory hub wherein there are two sizes of memory location in the first memory arranged in two said blocks, one of a size to receive relatively small data portions and the other of a size to receive relatively large data portions, and wherein data portions that are too large to be stored in a single memory block are stored as linked lists in a plurality of blocks (¶0007- ¶0008, wherein a large packet switch comprises several port cards and a switch fabric. The port cards in the large packet switch differ in a number of details from the port cards of the small packet switch. In the large packet switch, there is no single shared packet memory (as in the small packet switch); rather, each port card contains a separate packet memory which corresponds to two sizes of memory location in the first memory arranged in two said blocks, one of a size to receive relatively small data portions and the other of a size to receive relatively large data portions, and wherein data portions that are too large to

be stored in a single memory block are stored as linked lists in a plurality of blocks). with pointers pointing to the next block but without any pointers pointing from one data portion to the next data portion of the packet (¶0071 wherein recognizing the segmentation of packets provides switching behavior (selective read) rather than FIFO behavior to keep track of cell storage locations; ¶0078, fig7, wherein multi-cell pointer management structure each corresponding to pointers pointing to the next block but without any pointers pointing from one data portion to the next data portion of the packet).

Regarding claim 11, Van Asten discloses the sizes of the memory locations in the blocks are matched to the most commonly occurring sizes of data packets in the communication system (¶0013, wherein the fixed size packets (cells) correspond to the most commonly occurring sizes of data packet, since they are commonly set to the fixed size, and wherein the packet memories based on the cell size corresponds to the memory location in the blocks matching the commonly occurring sizes of the data packets).

Regarding claim 12, Van Asten discloses allocating the memory locations in said first memory from a pool of available addresses provided to it in batches from a central pool of available addresses (¶025, wherein the memory address being selected from a sub-set, i.e. pool, of N memory addresses corresponds to allocating the memory locations in said first memory from a pool of available addresses provided to it in batches from a central pool of available addresses).

Regarding claim 13, Van Asten discloses memory blocks segregated into a plurality of memory channels, the method further comprising allocating addresses to data portions sequentially across channels whereby to spread the storage of data portions across the channels (¶0030, wherein the number of memory modules in the plurality of N memory modules may vary depending on the application and is equal to N=5 in the embodiment of the invention wherein the variable size packet may be divided into different number X of cells depending on the cell size, conveniently X ranging from X=1 to about 200 corresponds to memory blocks segregated into a plurality of memory channels, the method further comprising allocating addresses to data portions sequentially across channels whereby to spread the storage of data portions across the channels).

Regarding claim 14, Van Asten discloses reading the data portions from the first memory in pipelined manner by a data retrieval unit adapted to instruct a memory block to read out a data portion without having to wait for the previous read to be completed, and releasing the address location from the first memory (¶0170, fig.8, wherein providing a pipelined system comprised of the read queues 608, read command queues 610, and the associated control logic in the read-write control 300 permits many switch cells to be requested and retrieved from the DRAM storage in parallel and re-ordered in separate queues, without stalling the flow of cells so that the read operation is not a single pipeline of requests and switch cell deliveries, but multiple pipelines are running in parallel corresponds to reading the data portions from the first memory in pipelined manner by a data retrieval unit adapted to instruct a memory block to read out a data

portion without having to wait for the previous read to be completed, and releasing the address location from the first memory).

Regarding claim 15, Van Asten discloses a large packet switch, the bandwidth available through the switch fabric usually greater than the bandwidth of the line interface in the port card, in order to accommodate the fluctuating packet traffic without the loss of packets. Van Asten does not expressly disclose an overflow situation when there is insufficient memory for a received packet wherein the data portion is discarded. However, Rege claims discarding one of said data packets when said one of said data packets is received and said packet buffer memory has insufficient free space to store said one of said data packets and a discard counter, i.e. record portion, to store a discard count of the number of said data packets that are discarded, see claim 9, for the purpose handling an inevitable situation of overflow.

Regarding claim 16, Van Asten discloses reading the address locations from a bitmap of addresses (fig. 10-806, wherein get next read command address A, count K corresponds to reading the address locations from a bitmap of addresses) when a memory location is released after the data stored therein has been read out (fig. 10-818, wherein release MCP corresponds to memory location is released after the data stored therein has been read out, i.e. cell put on read queue, fig. 10-812), the address of the released memory location is sent directly to the pool (fig. 10-818, wherein address is placed on a free list corresponds to the address of the released memory location is sent directly to the pool).

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Welin, Andrew M. (US 20020031086 A1), Minkenberg, Cyriel (US 20020064156 A1) Luijten, Ronald P. et al. (US 20020118689 A1), Anvar, Ali et al. (US 20030179644 A1), Luijten, Ronald P. et al. (US 20010021174 A1), Barnes; Peter M. et al. (US 7382787 B1), Ha, Sang-Hyuck et al. (US 20040117715 A1), Wong; Sau C. (US 6662263 B1), Clark; Paul H. et al. (US 5187780), Nichols; Stacy W. et al. (US 6314489 B1), Ren; Jing-Fei et al. (US 6160814), Beshai; Maged E. (US 6356546 B1).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to MAXWELL A. CLARK whose telephone number is (571) 270-1956. The examiner can normally be reached on Monday through Thursday 7:30A.M. to 5P.M. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

June 24, 2008

/Maxwell A. Clark/
Examiner, Art Unit 2616
/Huy D. Vu/
Supervisory Patent Examiner, Art Unit 2616